RELEASED

RFD2T5N200-702

RFuW Engineering Pte. Ltd.

SP2T PIN Switch Driver – Positive & Negative Voltage Driver

Features:

- Supports High Output Drive Voltage and Current
- Support MSW2T Series of High Power Switches
- Operates from +5V and -15V to -200V
- High Output Current (50 mA) for Low Loss and High Isolation
- Single TTL Input Control, Two Driver Outputs
- RoHS Compliant

Description:

The RFD2T5N200-702 surface mount PIN Switch Driver supports high biasing voltages required when operating PIN diodes at high frequencies. The fundamental building block consists of a PIN Diode and it is the intrinsic layer which gives this device its unique characteristics. When charge is injected into the intrinsic layer it becomes highly conductive and when charge is depleted from the intrinsic layer it becomes nonconductive. As the operating power increase or the frequency of interest drops into the HF & VHF realms, the necessary biasing voltages climb into the hundreds of voltage which exceeds the capabilities of all MMIC style Switch Drivers.

This device has been designed to support optimum biasing voltages required to support SP2T switch offering requiring both positive and negative biasing voltages. The RFD2T5N200-702 operates with a positive bias voltage of +5V and a negative voltage between -15V to -200V.

The RFD2T5N200-702 driver can source up to -100mA from the negative source and up to +50mA from the +5V supply. The driver is controlled via an independent TTL control signals. There are two complimentary outputs to support the typical Series-Shunt PIN diode switch topology.

The RFD2T5N200-702 is packaged in a 33mm x 33mm x8.4mm surface mount package. The device is compatible with surface mount, solder reflow processes typically employed in high volume production.

Environmental Capabilities

The RFD2T5N200-702 Driver is capable of meeting the environmental requirements of MIL-STD-202 and MIL-STD-750.

ESD and Moisture Sensitivity Rating

The ESD rating for this device is Class 1A, HBM. The moisture sensitivity level rating is MSL1.

Absolute Maximum Ratings

T_A= +25ºC as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Input Voltage, $+V_{CC}$		-0.1 to 5.5 V
Input Voltage, $-V_{EE}$		0.1 to -210 V
Control Port Input Voltage		-0.5 to 5.5 V
$-V_{EE}$ Output Sink Current	V_{OUT} ~ $-V_{EE}$ V	-125 mA
$+V_{CC}$ Output Source Current	V_{OUT} ~ $+V_{CC}$ V	+60 mA
Operating Temperature		-40ºC to 85ºC
Storage Temperature		-65ºC to 150ºC
Assembly Temperature	T < 10 sec	+260ºC
Total Dissipated Power	T_{CASE} = 85ºC	6.0 W

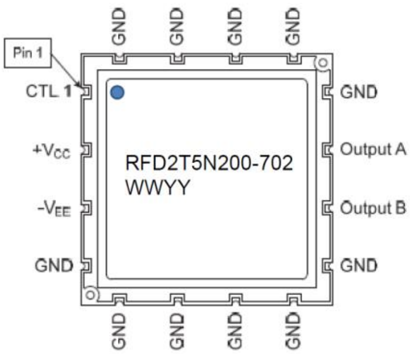
Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

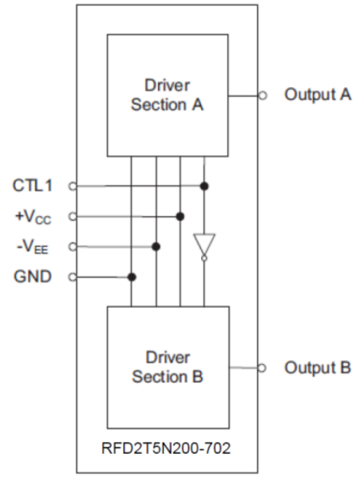
RFD2T5N200-702 Electrical Specifications

@ Z_o=50Ω, TA= +25ºC as measured on the base ground surface of the device.

Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Operating Frequency	PRF		0	100	500	KHz
Supply Voltage	$+V_{CC}$		4.5	5	5.5	V
Supply Voltage	$-V_{EE}$		-15	-50	-200	dB/ºC
Quiescent Current ($+V_{CC}$)	I_{Q1}	$+V_{CC}$=5V, $-V_{EE}$=-15V to -200V, No load connected to output A & B	10	20	30	mA
Quiescent Current (=V_{EE})	I_{Q2}	$+V_{CC}$=5V, $-V_{EE}$=-15V to -200V, No load connected to output A & B	-15	-25	-40	mA
TTL Input Voltage	V_{LOW} V_{HIGH}	Logic 0 Logic 1	0 2		0.8 5.0	V
Low Level Output Voltage Output A, B or C	V_{OUTL}	$+V_{CC}$=5V, $-V_{EE}$=-15V to -200V, Source current from $+V_{CC}$=50mA	$+V_{CC}$ -1	$+V_{CC}$ -0.5	$+V_{CC}$ -0.1	V
Low Level Output Voltage Output A, B or C	V_{OUTH}	$+V_{CC}$=5V, $-V_{EE}$=-15V to -200V, Sink current from $-V_{EE}$= 50mA	$-V_{EE}$ +1	$-V_{EE}$ +0.5	$-V_{EE}$ -1	V
Switching Time	T_{SW}	$+V_{CC}$=5V, $-V_{EE}$=-15V to -200V, F =10kHz, 50% TTL to 10% or 90% RF output voltage		1.5	2	usec

RFD2T5N200-702 Pin Out





Pin Out Description

Pin	Pin Name	Input/Output	Description
1	CTL1	I	TTL input control (CTL1)
2	$+V_{CC}$	I	+5V supply voltage input
3	$-V_{EE}$	I	Negative high voltage (-15 to -200V) input
4	GND		$+V_{CC}$ & $-V_{EE}$ ground return
5	GND		$+V_{CC}$ & $-V_{EE}$ ground return
6	GND		$+V_{CC}$ & $-V_{EE}$ ground return
7	GND		$+V_{CC}$ & $-V_{EE}$ ground return
8	GND		$+V_{CC}$ & $-V_{EE}$ ground return
9	GND		$+V_{CC}$ & $-V_{EE}$ ground return
10	Output B	O	Bias voltage/current output from driver port B
11	Output A	O	Bias voltage/current output from driver port A
12	GND		$+V_{CC}$ & $-V_{EE}$ ground return
13	GND		$+V_{CC}$ & $-V_{EE}$ ground return
14	GND		$+V_{CC}$ & $-V_{EE}$ ground return
15	GND		$+V_{CC}$ & $-V_{EE}$ ground return
16	GND		$+V_{CC}$ & $-V_{EE}$ ground return

Truth Table

CTL1 (notes 1 & 2)	Driver Output Section A	Driver Output Section B
V_{HIGH}	$V_{OUT}=+V_{CC}$ V, current sourcing mode	$V_{OUT} \sim -V_{EE}$ V, Current sinking mode
V_{LOW}	$V_{OUT} \sim -V_{EE}$ V, Current sinking mode	$V_{OUT}=+V_{CC}$ V, current sourcing mode

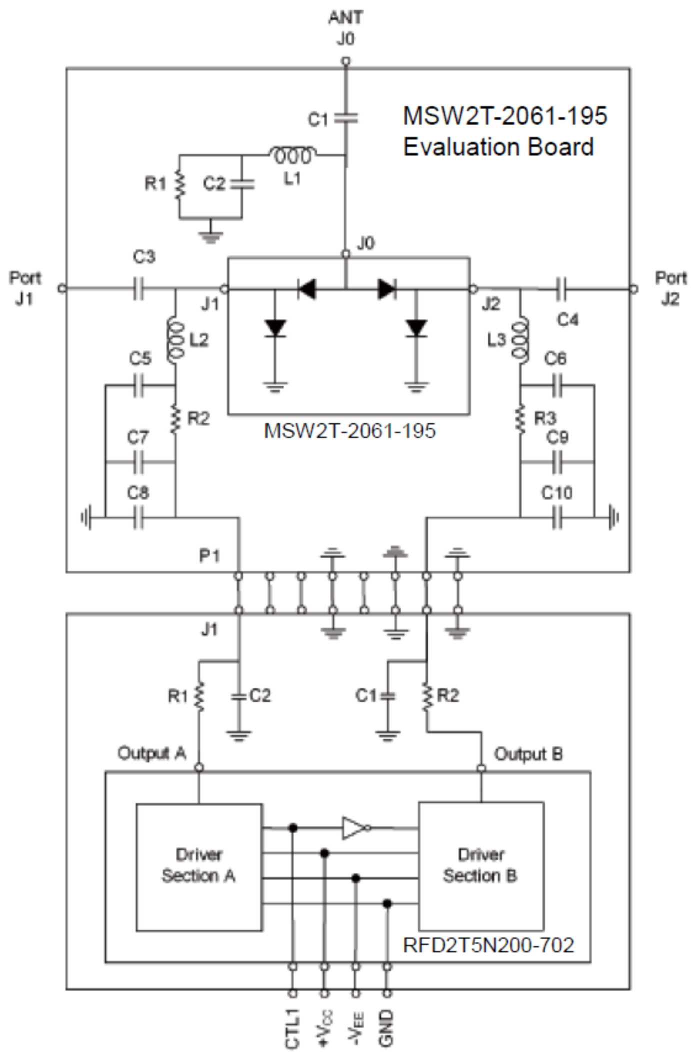
Notes:

1) $2V \leq V_{HIGH} \leq 5V$
2) $0V \leq V_{LOW} \leq 0.8V$
3) Not recommended state

Control of Symmetrical SP2T Switch

The RFD2T5N200-702 can control a symmetrical SP2T series-shunt PIN Diode switch. Each driver section is connected to one series-shunt switch element to provide biasing voltages required in the two operating states: RF State 1 and 2. The RF State of the SP2T is determined by the inputs to the Control signals: CTL1. The Control signal states drives the SP2T into a state where one port is in the Low Loss state while the other port is in the Isolation state.

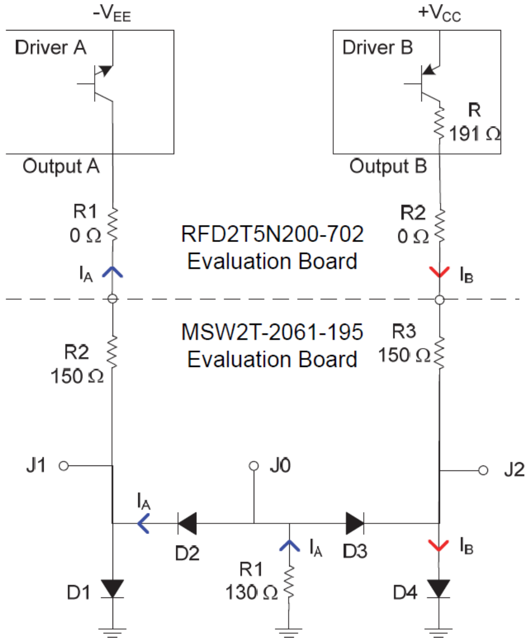
CTL1	RF State	Path J0 to J1	Path J0 to J2	Output A J1 Bias	Output B J2 Bias
LOW	1	Low Loss	High Isolation	V_{OUT} ~ $-V_{EE}$, Current sink mode	V_{OUT}~($+V_{CC}$ – I_{OUT} x 191)V, current source mode
HIGH	2	High Isolation	Low Loss	V_{OUT}~($+V_{CC}$ – I_{OUT} x 191)V, current source mode	V_{OUT} ~ $-V_{EE}$, Current sink mode



Positive & Negative Voltage PIN Diode Switch Driver

RF State 1

The schematic shown below reflect RF State 1 for the RFD2T5N200-702 driver interconnected to a SP2T evaluation board.



In RF State 1, the voltage from Output A of Driver A is approximately equal to $-V_{EE}$ supply voltage. This provides forward bias to the series PIN diode, D2, between the J0 and J1 ports. The magnitude of the resultant bias current through D2 is primarily determined by the output voltage from Output A, the magnitude of the forward voltage across D2 and the sum of the resistance of R1 and R2 on the SP2T evaluation board and R1 on the driver evaluation board. This current is nominally -100 mA.

At the same time, the PIN diodes D4 connected between J2 and ground is also forward biased by voltage produced at Output B which is slightly less than $+V_{CC}$ due to the voltage drop across the 191Ω internal resistors. Under this condition, the PIN diodes, D3 connected between the J0 and J2 ports are reverse biased. The magnitude of the bias currents through D4 is primarily determined by $+V_{CC}$, the magnitude of the forward voltage across D4 and the sum of the resistance of R3 on the switch eval board, R2 on the driver evaluation board and the 191Ω internal resistor. Nominally this current is 15mA.

The series PIN diodes, D3, must be reverse biased during RF State 1. The reverse bias voltage must be sufficiently large to maintain this diode in its non-conducting, high impedance state when a large RF signal voltage may be present in the J0 to J1 path. The reverse voltage across D3 is the arithmetic difference of the potentials at its anode and cathode.

The potential at D3's cathode is equal to the forward voltage of D4. These voltages are nominally 0.8V.

The potential at D3's anode is equal to the voltage drop across R1 of the SP2T eval board. This voltage is the product of the current through D2 and the resistance of R1. The voltage across D3 is given by:

$$V_{D3} = V_{ANODE\ D3} - V_{CATHODE\ D3} = V_{ANODE\ D3} - 0.8$$

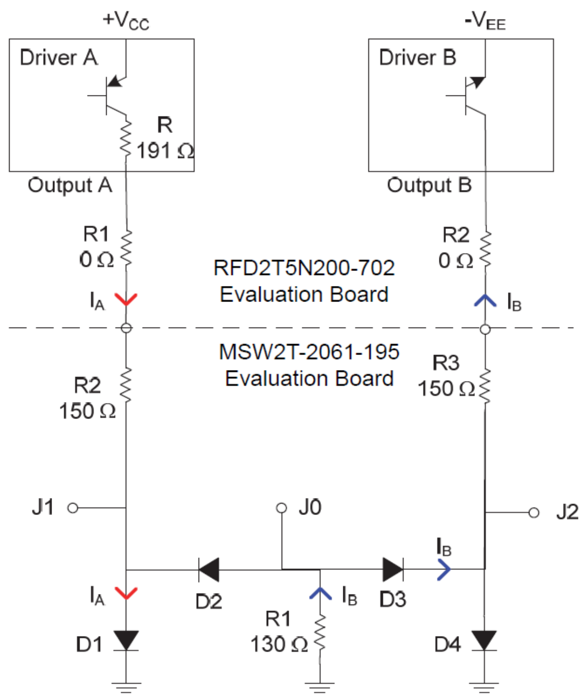
$V_{ANODE\ D3} = I_A \times R1 = [(-V_{EE} + VD2)/(R1 + R2)] \times R1 \sim [(-28 + 0.8)/280] \times 130 = -12.6V$

$V_{D3} = V_{ANODE\ D3} - V_{CATHODE\ D3} = -12.6 - 0.8 = -13.4V$

The minimum voltage required to keep D3 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the D3 anode, the frequency of the RF signal and the characteristics of the series diode, among other factors. The minimum required voltage can be calculated as described in the section "Minimum Reverse Bias Voltage".

RF State 2

The simplified DC Bias circuit schematic for RF State 2 for the RFD2T5N200-702 driver connected to the SP2T evaluation board is shown below:



In RF State 2, the voltage from Output B of Driver B is approximately equal to the $-V_{EE}$ supply voltage. This provides a forward bias to the series PIN diode, D3, between the J0 and J2 ports. The magnitude of the resultant bias current through D3 is primarily determined by the output voltage from Output B, the magnitude of the forward voltage across D3 and the sum of the resistances of R1 and R3 on the SP2T eval board and R2 on the driver evaluation board. This current is nominally -100 mA.

The magnitude of the bias current through D1 is primarily determined by +Vcc, the magnitude of the forward voltage across D1 and the sum of the resistances of R2 on the SP2T Evaluation Board , R1 on the Driver Evaluation Board and the internal 191Ω resistor. This current is nominally 15 mA.

The series PIN diodes, D2 must be reversed biased during RF State 2. The reverse bias voltage must be sufficiently large to maintain this diode in its non-conducting, high impedance state when a large RF signal voltage may be present in the J0 to J2 path. The reverse voltage across D2 and the diode D5 is the arithmetic difference of the potentials at their anode and cathode terminals.

The potential at D2's cathode is equal to the forward voltage of D1. This voltage is nominally 0.8V. The potential at D2's anode is equal to the voltage drop across R1 of the SP2T eval board. The voltage is the product of the current through D3 and the resistance of R1. The voltage across D2 is given by the following:

$$V_{D2} = V_{ANODE\ D2} - V_{CATHODE\ D3} = V_{ANODE\ D2} - 0.8$$

$$V_{ANODE\ D2} = I_B \times R1 = [(-V_{EE} + V_{D3})/(R1 + R2)] \times R1 \sim [(-28 + 0.8)/280] \times 130 = -12.6V$$

$$V_{D2} = V_{ANODE\ D2} - V_{CATHODE\ D2} = -12.6 - 0.8 = -13.4V$$

The minimum voltage required to keep the diodes D2 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at anodes of D2, the frequency of the RF signal and the characteristics of the series diodes, among other factors. The minimum required voltage can be calculated as described in the section "Minimum Reverse Bias Voltage".

Calculation of Resistor Values

The magnitude of the forward bias current applied to the series diode is set by the magnitude of the supply voltage –VEE, which is nominally 28V, the value of resistors R1 and R2 or R3 on the SP2T evaluation board as well as R1 on the driver evaluation board, the forward of the series diode, V_{DIODE}, among other factors. Given the desired currentvalue, the resistance is given by the following formula:

$$R_{TOTAL} = R_{\text{1 or 2(driver board)}} + R_{\text{1 (SP2T eval board)}} + R_{\text{2 or 3(driver board)}} = (-V_{EE} - V_{DIODE})/ I_{BIAS}$$

The magnitude of the current through the shunt diode is set by the magnitude of the supply voltage +Vcc, the value of resistance in series with the shunt diode (the internal 191Ω resistor, R1 or R2 of the driver board and R2 or R3 of the SP2T Evaluation Board) and the forward voltage of the shunt diode, VDIODE, among other factors. Given the desired current value, this resistance is given by the formula:

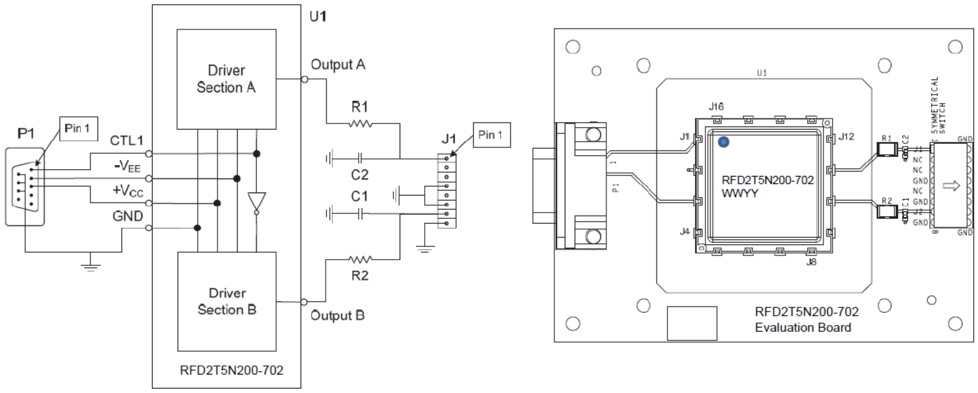
$$R_{SHUNT} = R_{\text{1 or 2(driver board)}} + R_{\text{2 or 3(driver board)}} + 191\Omega = (+V_{cc} - V_{DIODE})/ I_{BIAS}$$

Minimum Reverse Bias Voltage

$$|V_{DC}| = \frac{|V_{RF}|}{\sqrt{1 + \left[\left(\frac{0.0142 \times f_{MHz} \times W_{mils}^2}{V_{RF} \times \sqrt{D}}\right) \times \left(1 + \sqrt{1 + \left(\frac{0.056 \times V_{RF} \times \sqrt{D}}{W_{mils}}\right)^2}\right)\right]^2}}$$

The minimum reverse bias voltage required to maintain a PIN diode out of conduction in the presence of a large RF signal given by the following variables:

$\lvert V_{DC} \rvert$	= magnitude of the minimum DC reverse bias voltage
$\lvert V_{RF} \rvert$	= magnitude of the peak RF voltage(including the effects of VSWR)
f_{MHz}	= lowest RF signal frequency expressed in MHz
D	= duty factor of the RF signal
W_{mils}	= I region thickness of the PIN Diode (expressed in mils)



The RFD2T5N200-702 evaluation board contains several passive components. R1 and C2 are optional components which may be used to shape the output signal of Output A. Likewise, R2 and C1 may be used to shape the output signal from Output B. C1 and C2 capacitors are normally not installed. R1 and R2 are installed with 0Ω, 0.5W resistors. The positive supply voltage, nominally 5V, is designated as $+V_{CC}$. The negative supply voltage, nominally -15V to -200V, is designated as $–V_{EE}$.

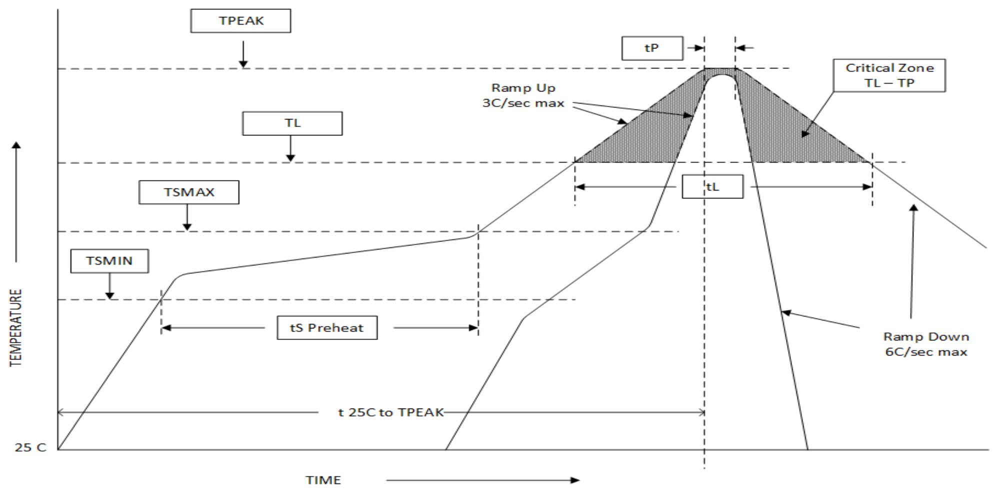
There are two multi-pin connectors on the board. P1 is a DB-9 male connector which facilitates connection of the TTL control signal, supply voltages and ground to the evaluation board. Symmetrical switch is a 16 pin female header which can be used to connect directly to the male header on the symmetrical SP2T Evaluation Board. The pin out for these connectors are shown below:

Assembly Instructions

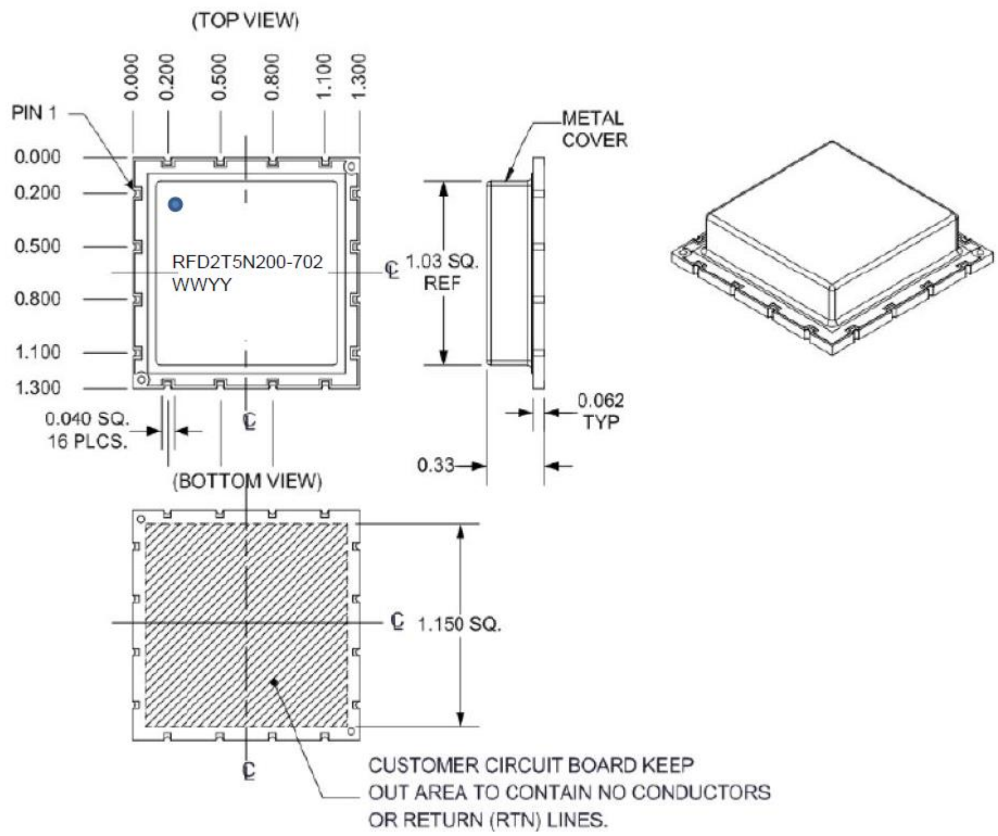
The RFD2T5N200-702 may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat Temp Min (T_{smin}) Temp Max (T_{smax}) Time (min to max) (t_s)	 100°C 150°C 60 – 120 sec	 100°C 150°C 60 – 180 sec
T_{smax} to T_L Ramp up Rate		 3°C/sec (max)
Peak Temp (T_P)	225°C +0°C / -5°C	260°C +0°C / -5°C
Time within 5°C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above: Temp (T_L) Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T_P	6 minutes (max)	8 minutes (max)

Solder Re-Flow Time-Temperature Profile



RFD2T5N200-702 Package Outline Drawing



Notes:

1) Circuit Board material is FR4.
2) Metallization: 2 0z Cu followed by 150uin (TYP), followed by 4uin (TYP) Au
3) Unit = inches

Part Number Ordering Detail:

The RFD2T5N200-702 PIN Switch Driver is available in the following format:

Part Number	Description	Packaging
RFD2T5N200-702	SP2T Positive & Negative Voltage Switch Driver	Gel-Pack
RFD2T5N200-702-EVB	RFD2T5N200-703 Evaluation Board	Box